

GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION
SPONSORED PROJECT INITIATION

Date: 1/12/81

Project Title: STINGER-POST Simulation Validation Preparation

Project No: A-2826

Project Director: Mr. C. E. Barnett

Sponsor: U. S. Army Missile Command; Redstone Arsenal, AL 35898

Agreement Period: From 12/9/80 Until 6/1/81 (Perf.)
8/1/81 (Rpts.)

Type Agreement: Delivery Order No. 0001 under Contract No. DAAH01-81-D-A003

Amount: \$96,365.40

Reports Required: Final Technical Report

Sponsor Contact Person (s):

Technical Matters

Dr. M. M. Hallam
Systems Simulation & Development
Directorate
U. S. Army Missile Command
ATTN: DRSMI-RDF
Redstone Arsenal, AL 35898
205/876-4141

Contractual Matters

(thru OCA)

Mr. Thomas A. Bryant
ONR Resident Representative
Georgia Institute of Technology
206 O'Keefe Building
Atlanta, GA 30332

Defense Priority Rating: D0-A2 under DMS Reg 1

Assigned to: EML/RSD

(School Laboratory)

COPIES TO:

Project Director
Division Chief (EES)
School/Laboratory Director
Dean/Director-EES
Accounting Office
Procurement Office
Security Coordinator (OCA)
~~Reports Coordinator (OCA)~~

Library, Technical Reports Section
EES Information Office
EES Reports & Procedures
Project File (OCA)
Project Code (GTRI)
Other _____

SPONSORED PROJECT TERMINATION SHEETDate 9/28/81

Project Title: STINGER-POST Simulation Validation Preparation

Project No: A-2826

Project Director: Mr. C. E. Barnett

Sponsor: U. S. Army Missile Command; Redstone

Effective Termination Date: 6/1/81Clearance of Accounting Charges: 8/1/81 Reporting

Grant/Contract Closeout Actions Remaining:

- ☒ Final Invoice ~~and Closing Documents~~
- ☐ Final Fiscal Report
- ☐ Final Report of Inventions
- ☐ Govt. Property Inventory & Related Certificate
- ☐ Classified Material Certificate
- ☐ Other _____

Assigned to: EML/RSD (School/Laboratory)COPIES TO:

Administrative Coordinator
Research Property Management
Accounting
Procurement/EES Supply Services

Research Security Services
~~Reports Coordinator (OCA)~~
Legal Services (OCA)
Library

EES Public Relations (2)
Computer Input
Project File
Other Mr. Barnett - Huntsville

5B-227
FINAL REPORT DAAH01-81-D-A003/0001

PROJECT NO. A-2826

STINGER/POST SIMULATION VALIDATION PREPARATION

GEORGIA INSTITUTE OF TECHNOLOGY

A Unit of the University System of Georgia
Engineering Experiment Station
Atlanta, Georgia 30332



1981



June 1981

Prepared for

U.S. ARMY MISSILE COMMAND
REDSTONE ARSENAL, ALABAMA 35809

FINAL REPORT
EES/GIT Project A-2826

STINGER/POST SIMULATION VALIDATION PREPARATION

By

C. E. Barnett
T. N. Long

Contract No. DAAH01-81-D-A003
Delivery Order No. 0001

U. S. Army Missile Command
Redstone Arsenal, Alabama 35898

June 1981

GEORGIA INSTITUTE OF TECHNOLOGY
Engineering Experiment Station
Atlanta, Georgia 30332

PREFACE

This report was prepared by the Electromagnetic Laboratory of the Engineering Experiment Station, Georgia Institute of Technology. The project documented herein was directed by C. E. Barnett and was staffed by him, T. N. Long, and in its early phases by C. T. Wallace. Dr. M. M. Hallum, III, Chief, Systems Evaluation Branch, Army Missile Laboratory, U. S. Army Missile Command, was technical monitor and Mr. V. S. Grimes provided daily technical coordination. The valuable assistance provided by Messrs. D. Curry, R. Roberts, and T. Adams in the implementation of digital and analog programs was sincerely appreciated. The Electronic Target Signal Generator (ETSG) development continued under the guidance of M. Sinclair, J. Randolph and G. Loefer of EML/EOD. B. Burt and P. Pritchett of the University of Alabama in Huntsville maintained the ETSG and continued its development at Redstone Arsenal.

The technical viewpoints, opinions and conclusions expressed in this report are those of the authors and do not necessarily express or imply policies or positions of the U. S. Army Missile Command.

TABLE OF CONTENTS

	<u>Page</u>
1.0 INTRODUCTION.....	1
2.0 HYBRID SIMULATION STATUS.....	5
2.1 Analog Models and Control Logic Status.....	5
2.2 Electronic Target Signal Generator Status.....	8
2.3 Digital Program Status.....	11
2.4 Breadboard Status.....	12
2.4.1 Installation and Power-Up Procedure.....	12
2.4.2 Breadboard Tailoring Procedure.....	13
2.5 HISC and Interface Status.....	13
3.0 INTEGRATED VALIDATION PREPARATION.....	18
3.1 Detector Channel Noise Minimization.....	18
3.2 Validation Plan and Procedure.....	19
3.2.1 Integration Plan.....	20
3.2.2 Verification.....	21
3.2.3 Validation Procedure.....	21
4.0 CONCLUSIONS AND RECOMMENDATIONS.....	22
REFERENCES.....	24
Appendix A Operation Sequence for Installation of the Stinger/POST Breadboard into the Hybrid Simulation.....	A-1
Appendix B Breadboard Precursory Checks Required for MICOM Simulation.....	B-1
Appendix C Breadboard Tailoring Procedures Required for MICOM Simulation.....	C-1
Appendix D Hybrid Simulation Integration Plan.....	D-1

LIST OF FIGURES

<u>Number</u>	<u>Title</u>	<u>Page</u>
2-1	Stinger/POST Gyroscope Model Analog Diagram.....	6
2-2	MICOM Hybrid Simulation Facility Trunking for Stinger/POST Simulation.....	17
3-1	Commons Interconnection Configuration.....	18
4-1	Integration Schedule.....	D-15

LIST OF TABLES

<u>Number</u>	<u>Title</u>	<u>Page</u>
2-1	HISC-Breadboard Cable Wiring List.....	14
2-2	HISC-ETSG Interface Terminal Strip List.....	15
2-3	HISC Patching Instructions for Stinger/ POST Configuration.....	16

1.0 INTRODUCTION

The project documented in this report was accomplished during the period of 8 November 1980 to 1 June 1981. It was intended to verify performance of the Stinger/POST hybrid simulation, to define target and countermeasure scenarios in ETSG format and to develop procedures, data requirements and run matrices for validation of the Stinger/POST hybrid simulation. In addition, the delivery order called for verification and validation of software and firmware changes in the Stinger/POST CCMV Guidance Electronics Breadboard Assembly (BB) and in the ETSG through use of a Tektronix 8002 Microprocessor Development Laboratory (MDL). The simulation employed the ETSG, an EAI 781 Parallel Analog Processor, a CDC 6600 digital computer program and the Breadboard Assembly.

The project resulted in the definition of interface and tailoring procedures for the Stinger/POST Breadboard Assembly, the modification of the Hybrid Interface Signal Conditioner (HISC) to minimize excessive noise in the analog detector output channel from the ETSG to the Breadboard, the operation of the ETSG, and the integration of the Breadboard into the hybrid simulation. A simulation integration plan was developed, and a validation procedure was defined. The validation procedure was being implemented as the project performance period ended. Unrealized goals included the use of the MDL for Breadboard firmware analysis. ETSG software and hardware proved compatible with the MDL and several updates were instituted with it. Breadboard integration, tailoring and checkout were given priority over the disassembly and analysis of the firmware in that

unit. In addition, no Breadboard firmware updates or revisions were available for validation and verification.

The project was a continuation of a process to develop a hybrid simulation of the Stinger/POST missile for analysis of performance of the guidance system and prediction of the missile performance in a variety of target and countermeasure environments.

The ETSG was brought through the third phase of its manufacture, i.e., it was connected with the Direct Cell B and thereby the CDC 6600 digital computer. This permitted demonstrating end-to-end so that a digital target data upload produced an analog detector output. The first two phases comprised the ETSG assembly at Atlanta and the ETSG installation and continued development at Redstone Arsenal. Functional development was continuing at the end of the performance period. The ETSG was demonstrated to the target image memory map level in February and produced an analog output in April. The noise level in the signal commons of the BB, ETSG and HISC was sufficiently high to prevent use of the output until the HISC was modified to mutually isolate the signal commons. Following that, the sensor output was applied to the Breadboard. Successful complete integration awaited integration of the analog gyro model and Breadboard.

The analog models were relocated from the AD-4 analog computer to the EAI 781 parallel analog processor during the initial phases of the

performance period. The gyro, ideal seeker and wing servomechanism models were checked out in a stand-alone configuration as well as in conjunction with the digital airframe and ideal seeker models. Following installation of Breadboard power supplies and verification of HISC interconnection, the integration of the analog gyro model and the Breadboard was begun. Gyro speed control circuitry in the Breadboard successfully controlled the gyro, and launch sequencing logic was integrated with the Breadboard. Manual modes were added to the analog logic to support extended pauses in the sequence.

The digital software was exercised in a real-time, stand-alone configuration as well as while integrated with the analog ideal seeker and gyro models. The digital target trajectory tables were extended into the prelaunch period of the simulation so that target tracking during the prelaunch sequence could be modeled.

Power supplies for the Breadboard were installed in the ETSG cabinets and the Breadboard was powered up for checkout. MICOM tailoring procedures were developed as required because the hybrid simulation installation was different from that of the missile contractor. Gyro integration and function verification was begun. Following some Breadboard repairs, gyro speed control was supplied successfully.

The integration of the ETSG and Breadboard into the hybrid simulation was suspended in March for about a month because detector channel noise was too high for initial Breadboard setup. Noise minimization techniques were

devised and implemented in the HISC. Following this, the procedures resumed as laid out in the Integration Plan.

The status of each simulation component system is addressed in Section 2.0 of this report and the integration and preparation for validation are discussed in Section 3.0. The summary of results and the description of remaining procedures and problems are covered in Section 4.0.

2.0 HYBRID SIMULATION STATUS

The hybrid simulation was being integrated as of 1 June 1981, but several problems remained to be solved before validation could begin. This section deals with the status of each simulation component system.

2.1 Analog Models and Control Logic Status

The gyroscope model was verified as accurately modeling the dynamics equations following the implementation on the EAI 781 analog processor but dynamic analysis could be analyzed only in a limited way until the Breadboard became available. The digital program and analog models of the gyro and ideal seeker were combined in a short version of the real-time closed loop in March and stable gyro operation was observed during precursor sweep tests and the GTV-1 preflight conditions. The ideal seeker generated precession commands for the gyro model but the wing servo-mechanism model was not included. Simulated flight times were within 50 ms of the times predicted by the missile contractor.

Following availability of the Breadboard, signal level matching was accomplished by adjusting analog computer potentiometers to provide stable and predictable responses to the gyro speed control signals and the Breadboard precision command. A sign error existed at an output from Resolver R520, the Hooke-hinge-effect generator, causing an incorrect sum of roll rate and gyro spin frequency to be generated by Resolver R510 (Figure 2-1). Following this correction and some adjustment of

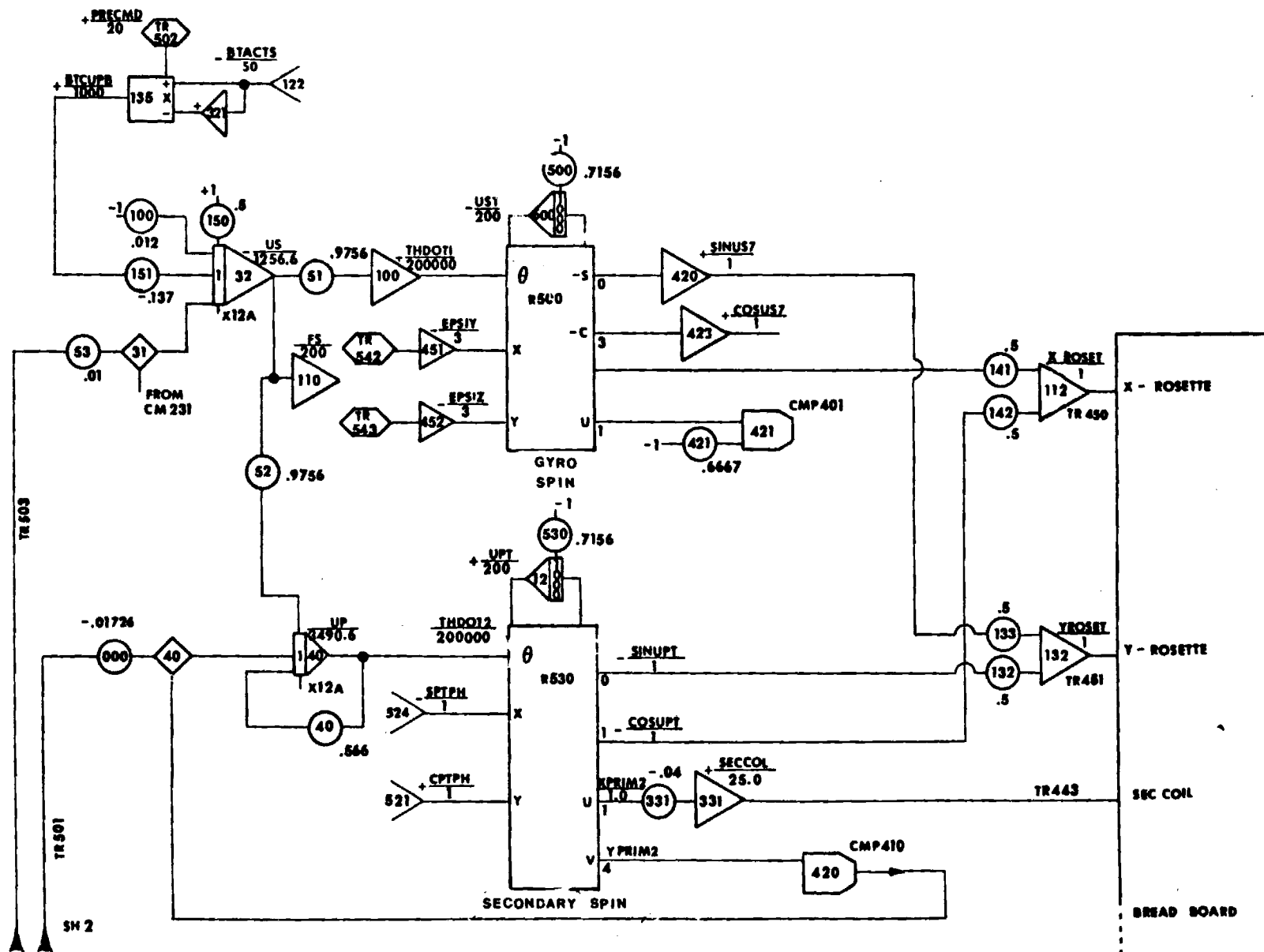


Figure 2-1. Stinger/POST Gyroscope Model Analog Diagram (Sheet 1 of 2)

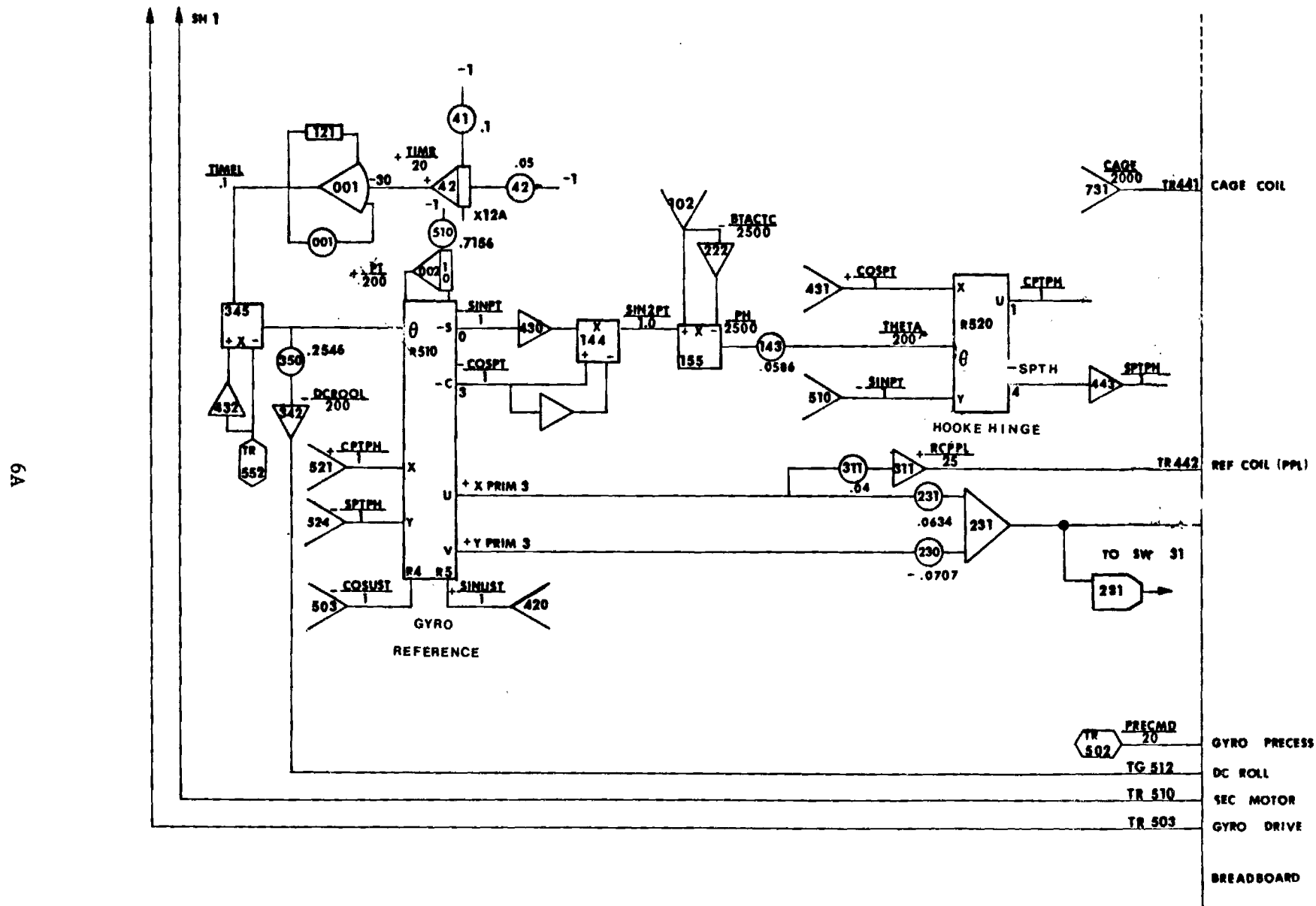


Figure 2-1. Stinger/POST Gyroscope Model Analog Diagram (Sheet 2 of 2)

potentiometer 000 to optimize the voltage of the gyro speed control signal from the Breadboard, gyro speed control was accomplished on 27 May. The initial setting for this potentiometer had to be doubled so that the post-launch gyro stable speed would be attained at the same rate as observed on the GTV-1 test flight.

The model initially failed to cage during Caged mode because of lack of an active Precession command from the Breadboard. Two malfunction mechanisms were identified: a malfunctioning voltage regulator in the Breadboard was preventing a relay from picking and the Cage-In signal to the Breadboard guidance connector from the HISC was not being provided to the circuitry which formed the Precession command. The regulator was replaced with satisfactory results but the implication of the open circuit and the optimal workaround method were undefined at the end of the performance period. The gyro could be effectively caged manually from the Breadboard front panel switch.

Control logic was checked out through the logic trunking stations and buffer networks and manually controlled flip-flop switches were provided for Gyro Operate, Gyro Cage and Launch command signals. These allowed checkout of the analog models and Breadboard responses without requiring that the digital program be run.

2.2 Electronic Target Signal Generator Status

During the period of performance of this delivery order, the ETSG progressed from a set of components still being assembled to a state of integrated development. The ETSG hardware was transported to the Missile Laboratory in July 1980 and initial component checkout proceeded through November. New cables and printed-circuit board edge supports were installed to improve electrical connection reliability and a diagnostic printed-circuit board was provided in each card cage so that image plane graphics were available to aid in maintenance and checkout. Additionally, packaging was reconfigured to provide more effective cooling to heat sensitive components.

The DCB interface was verified early in the period allowing target parameter loading directly from the CDC 6600 digital program. This allowed precise control of dynamic targets so that integrated checkout of target software could begin. Several software design problems became evident. Among these were the inadvertent reversal of J and K target channels so that J targets showed up in the K channel and vice versa, the invisibility of targets at ranges greater than resolution range and the inconsistency of aspect definitions for plane and complex targets.

The channel interchange problem was by-passed using the Initialization Processor's monitor program until a permanent solution was implemented. The range problem was corrected with firmware and software changes following extensive analysis with the recently acquired Microprocessor Development System. The aspect definition was such that the aspect

value for a side view of a complex target would cause an edge view for a plane target. Two solutions were possible: the digital program could keep track of target type and send the appropriate aspect cosine; or the ETSG firmware could be changed so that a given aspect cosine would be consistent for both. The implication of an ETSG firmware change was not fully known. Changes of this nature were approached with caution because of the interdependence of calculations within the firmware. Accordingly, the digital program bookkeeping solution has been instituted and will be retained until the details of an ETSG solution can be completed.

The majority of the conceptual design and specific hardware implementations proved successful. The target/pixel mapping algorithms provided a straightforward though complicated hardware realization. Because of this complication, the target loaders each contain 24 high speed ALU's which will be difficult to troubleshoot should problems occur. Either very extensive diagnostic software needs to be developed for this maintenance or a sufficient quantity of spares must be made available.

Another area of concern is in the direct memory assessing of the target CPU's. Some reliability problems have been encountered in this area where the target CPU's occasionally will not halt or unhalt. The conditions under which this occurs are not exactly known and may require future attention should it cause a degradation in system performance. A major effort should also be directed toward improving the mechanical and electrical integrity of the card cages as these have caused and will continue to cause reliability problems due to electrical/mechanical contact failures.

The ETSG hardware was designed with extensive diagnostic interfaces to facilitate maintenance. At present, only crude operator interfacing is available through the console as extensive diagnostic software was not a part of the contractual agreement. With a thorough knowledge of the ETSG hardware hierarchy, the operator is capable of exercising any major module or submodule through the console. A test input can be applied to a module and its output intercepted to verify its integrity. Various diagnostic programs written in "Basic" have been supplied that will create general purpose targets and exercise their static (polarity, strobe designation, and channel assignment) and dynamic parameters (range, aspect and orientation angle, azimuth, and elevation) through all modules of the ETSG. The individual target CPU's each contain built-in diagnostic firmware in the form of a generalized target exercising full range and orientation capabilities. By setting the appropriate flag in the desired CPU, (through the console) the generalized target will be used to produce corresponding missile audio output, depending on the initialization parameters set.

A system of image-plane graphics has been provided to aid in maintenance and checkout. Each card cage contains a printed circuit board with bus termination resistors, static LED indicators, and two sets of XYZ digital-to-analog converters. The XYZ converters are jumpered to their respective backplane signals. Thus, signals can be displayed on an XYZ scope showing image plane targets out of the target loader module, into and out of each target map and into each digital-to-analog converter. This

graphic device has proved to be an invaluable qualitative tool in the testing and maintenance of the ETSG.

The future maintenance and reliability of the ETSG will depend on permanent solutions to the problems of the target CPU's unexpected halting and the uncertainty of the electrical contacts between the printed circuit cards and their respective backplanes. Extensive "turn-key" diagnostic software as well as a respectable inventory of working spares will assure minimum down time for the ETSG and ease of maintenance.

2.3 Digital Program Status

The digital program was prepared and maintained by D. M. Curry to satisfy requirements established in the execution of this and precursor delivery orders. The routines for the airframe model, target trajectory tables, an ideal seeker and several open-loop analysis models were prepared before this delivery order was activated. During this delivery order period, the airframe model interface scaling was modified to relate properly to the ETSG and target trajectory tables were extended backward into the prelaunch time period. This latter modification was performed to allow target tracking during the prelaunch sequence in preparation for a test series in the fourth quarter of this year.

At the end of the delivery order performance period only two targets, one for each of two channels, could be specified. Program changes had been defined to allow the specification of a total of six targets in two channels. Some of the targets will be flare models, requiring the

definition of relative trajectories. The amount of phase lead required in the target parameter loads during closed-loop operation has not been determined because the time delay of signal propagation through the ETSG has not been measured. It is planned that some lead will be added to target location and some will be added to the wing position provided by the analog servomechanism model in response to the Breadboard guidance command. This will be effected as an extrapolation. Validation procedures have been established for measuring the time delay which must be allowed for.

2.4 Breadboard Status

The Breadboard was used in an as-delivered condition with checkout and maintenance performed only when signal indications in response to established procedures were different than expected. Tailoring of the Stinger/POST CCMV guidance electronics Breadboard was performed, for the most part, at the missile contractor facility. This tailoring should be valid for usage in the MICOM hybrid simulation because care has been taken to maintain the same signal scaling at critical interfaces. There are three tailoring procedures, however, which must be performed before beginning each new series of runs with the Breadboard. These include the scan phase tailor, the signal-to-noise ratio adjustment, and the track phase tailor.

2.4.1. Installation and Power-Up Procedure

Installation instructions are outlined in Appendix A. Following installation, several precursor checks should be made before

attempting to tailor the Breadboard. These are outlined in Appendix B.

2.4.2 Breadboard Tailoring Procedures

The required tailoring procedures are then outlined in Appendix C.

2.5 HISC and Interface Status

Final design and implementation of the HISC and simulation interfaces has been completed for the Stinger/POST hybrid simulation configuration. Extensive testing has been performed also, with synthesized detector noise minimization being the only area which is foreseen as a possible stimulus for further modifications. Some of the documentation for the HISC and interfaces is included in the following pages. Table 2-1 provides the details of the cable which connects the Breadboard and the HISC. Table 2-2 provides the details of the terminal strips used to connect the ETSG and the HISC.

Instructions for patching the front panel of the HISC in the Stinger/POST configuration are outlined in Table 2-3. And finally, the required MICOM Hybrid Simulation Facility trunking is illustrated in Figure 2-2. Schematics of the HISC have received a complete update but had not been thoroughly checked at the time of the writing of this report. For this reason, they will be published at a later date.

TABLE 2-1

HISC - BREADBOARD CABLE WIRING LIST

Signal	HISC	Cable IW6		Breadboard	
	Connector Pin No.	Connector Pin No.	Connector Pin No.	Connector Pin No.	Front Pin No.
Precession Coil	P6 - 3	S6 - 3	P98 - 34	J98 - 34	31
Cage Coil	4	4	30	30	32
Secondary Reference	5	5	12	12	13
UV Preamp	6	6	8	8	16
Signal Return 1	7	7	28	28	1
Gyro Drive	9	9	16	16	33
IR AGC 1	13	13	20	20	40
Precession Return	22	22	36	36	42
Gyro Reference	23	23	26	26	10
IR Preamp	24	24	4	4	2
Preamp Return	25	25	24	24	21
Secondary Drive	28	28	14	14	36
IR AGC 2	32	32	10	10	42
Timer Start	1	1	P99 - 6	J99 - 6	76
Buffered Cage Coil	2	2	10	10	18
Signal Return 3	8	8	30	30	3
Guidance Command	10	10	36	36	26
UV Preamp/ Pulse Amp	11	11	4	4	14
TE Pulses/ IR Threshold	12	12	28	28	43
TAG/AGC Control	20	20	26	26	19
Cage-In	21	21	P75	None	75
Wing Erect Control	27	27	P99 - 34	J99 - 34	48
IR Preamp/ Pulse Amp	29	29	24	24	29
0+ Wing Erect/ UV Threshold	30	30	14	14	47
Audio/Sync Filter	31	31	12	12	27

TABLE 2-2

HISC-ETSG INTERFACE TERMINAL STRIP LIST

Signal	HISC ETSG I/O Connector-Pin No.	ETSG * Terminal Strip Block-Pin No.
IR Preamp (K Channel) +	J1 - 22	A-1
IR Preamp (K Channel) -	T	2
UV Preamp (J Channel) +	Y	3
UV Preamp (J Channel) -	16	4
IR Preamp AGC 1 (K1)	20	5
IR Preamp AGC 2 (K2)	W	6
UV Preamp AGC 1 (J1)	19	7
UV Preamp AGC 2 (J2)	X	8
HISC Common	Z	9
ETSG Run (User Discrete 2)	R	B-1
ETSG Ready (User Discrete 3)	14	2
User Discrete 7	12	3
User Discrete 6	N	4
User Discrete 5	13	5
User Discrete 4	P	6
Spin Clock (User Discrete 0)	17	7
CDC Interrupt (User Discrete 1)	U	8
ETSG Common	1	9
X-Rosette Scan	V	C-1
Y-Rosette Scan	18	2
Spare	--	3
Spare	--	4
Spare	--	5
Spare	--	6
Spare	--	7
Spare	--	8
Spare	--	9
* Terminal strips are labeled A-C from left to right and numbered 1-9 from bottom to top.		

TABLE 2-3

HISC PATCHING INSTRUCTIONS FOR STINGER/POST CONFIGURATION

From		To		Signal
Module	Pin No.	Module	Pin No.	
Discrete In A	2	B.B.P.P. *	4	Cage Command
Discrete In A	3	B.B.P.P.	1	Launch Command
Analog In	X	ETSG I/O	6	X-Rosette
Analog In	Y	ETSG I/O	7	Y-Rosette
Analog In	Cage	B.B.P.P.	11	Cage Coil
Analog In	Gyro	B.B.P.P.	12	Gyro Reference
Analog In	Sec	B.B.P.P.	13	Secondary Reference
B.B.P.P.	18	Analog Out	2	Wing Command
B.B.P.P.	15	Analog Out	3	Precession
B.B.P.P.	16	Analog Out	4	Gyro Drive
B.B.P.P.	17	Analog Out	5	Secondary Drive
B.B.P.P.	5	ETSG I/O	3	K AGC 1
B.B.P.P.	6	ETSG I/O	4	K AGC 2
ETSG I/O	1	B.B.P.P.	9	IR Detector
ETSG I/O	2	B.B.P.P.	10	UV Detector
HISC Power	Gnd	B.B.P.P.	2	Test Command
		B.B.P.P.	3	AGC Freeze Command
		Analog Out	Sig Gnd	
		Analog Out	**	
		Discrete Out	**	
<p>* Breadboard Patch Panel</p> <p>** All unused lines.</p>				

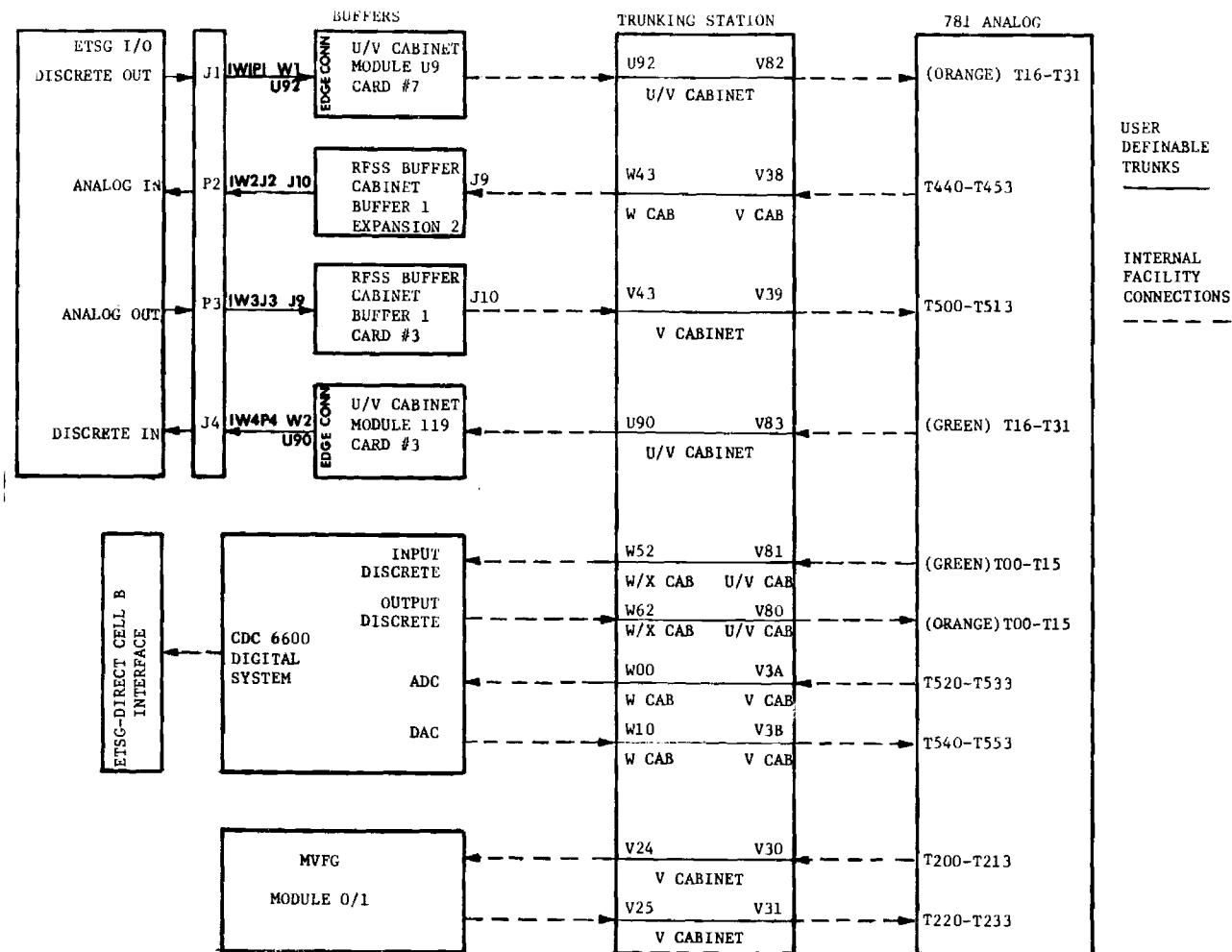


Figure 2-2. MICOM Hybrid Simulation Facility Trunking for Stinger/POST Simulation.

3.0 INTEGRATED VALIDATION PREPARATION

In completing the integration of the hybrid simulation, a detector noise problem was encountered which required resolution before further work could proceed. The problem is identified and the minimization procedure explained in Section 3.1. The verification plan and validation procedure are presented in Section 3.2.

3.1 Detector Channel Noise Minimization

Original simulation design provided for two separate commons. This could be thought of as two independent electronic systems connected differentially. One system consisted of the trunking stations, analog computer, etc., of the simulation facility. The other system consisted of the ETSG, HISC, and Stinger/POST Breadboard. However, noise measurements made at the "predetect" monitor points on the Breadboard indicated that a prohibitive amount of noise was present. In an attempt to improve the condition, the system was reconfigured with three commons as illustrated in Figure 3-1.

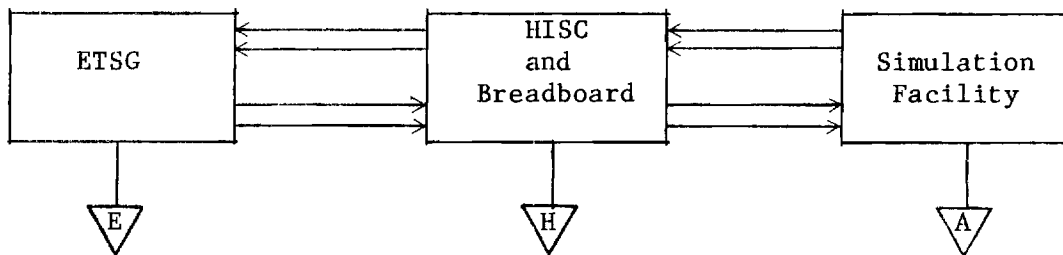


Figure 3-1. Commons Interconnection Configuration

The intent of this configuration is to separate ground noise generated by the ETSG from the HISC and Breadboard system.

Preliminary measurements indicate that major improvements were effected by the reconfiguration. Measurements made on several different dates were in the acceptable range, but at other times the noise level was unacceptable. Several details of the reconfiguration effort remain to be thoroughly checked though. However, new approaches may be required to complete the noise minimization effort.

3.2 Validation Plan and Procedure

Validation is defined as the procedure of comparing output from the logically correct simulation with missile flight test results. Two milestones must be accomplished before that process can begin: integration must be completed and verification must be satisfactorily completed. Integration is the completion of the simulation to the point that all signal interfaces are complete and signals procedure apparent satisfactory and stable reactions. Verification and validation tend to overlap but verification implies and includes the analysis and evaluation of component transfer functions.

3.2.1 Integration Plan

The integration of the gyroscope model with the Breadboard in terms of speed control and cage functions will be completed. This will be followed by Breadboard tailoring with the ETSG providing the requisite targets (Appendix D documents the preliminary plan prepared in February 1981). The principal area where the preliminary plan is no longer applicable pertains to the ETSG. Significant development of this component system has been realized and the system is supporting integration and verification of other systems. The wing servomechanism model response to Breadboard output will be assured, as well as the digital program response to wing angle changes provided by the servomechanism model. Movement of the target laterally at a constant range by the digital program, while the analog is in Operate and Breadboard is in POST mode should assure this interface. This should consume about five weeks, assuming no difficult malfunctions.

The transit time of a signal through the ETSG will be determined as a final step of integration. The digital program will position a target on boresight as an initial condition. The start of the timed run will be the removal of the target from the Field of View (FOV). The end of that delay time period will be the disappearance of the track pulse. The Visicorder optical recorder will be used to record the occurrence of the DCB transfer, as well as the output pulse string. A second test will monitor the movement of a target from boresight in a step to fifty percent

of the angle away from boresight to the edge of the FOV. Breadboard output will not be allowed to drive the gyro for this test.

3.2.2 Verification

Sweep and sled test correlation will be the principal components of verification. Simply stated, the process will not be quite so simple to implement. This should take better than a month.

3.2.3 Validation Procedure

Validation should be referenced to actual system performance data. Some data do exist characterizing the servomechanism, but none is available for other components. Validation will, therefore, depend largely upon matching flight test results. The GTV-1 flight results for the period starting at about two seconds into the flight will be used for initial validation. GTV-2 flight conditions will next be modeled.

4.0 CONCLUSIONS AND RECOMMENDATIONS

The integration of the hybrid simulation of the Stinger/POST missile system was proceeding at the end of the delivery order performance period. Several problems had been encountered and resolved and others were being defined with resolutions in process. The analog-computer model of the seeker gyroscope was being integrated with the Breadboard. Partial tailoring of the Breadboard was underway but signal-to-noise ratio setup could not proceed until the noise minimization procedures could be completely validated. The digital software was reconfigured to support minus-time tracking. The ETSG was used in an initial one-target, one-channel configuration and satisfactorily supported other integration activity. The lack of electrical interconnection integrity was a continuing problem but was manageable and should be minimized by the installation of new printed-circuit-card cages. The lack of user-oriented diagnostic software caused the isolation of some problems to be lengthy and circuitous.

Breadboard initialization and power-up procedures were defined and verified. Tailoring procedures were developed in preparation for integration of the Breadboard into the hybrid simulation. These procedures were being verified as the delivery-order performance period ended. Extensive modifications to the HISC grounding and common system were instituted to minimize missile audio signal noise. These changes had not been fully validated at the end of the period.

A validation plan was in place and verification procedures were being implemented to fully qualify the analog gyro model and signal interfaces throughout the simulation.

REFERENCES

1. GM6-255-3143, Stinger/POST CCMV Breadboard Operating Procedure, 13 February 1981, by M. L. Bellemare
2. TP6-255-4082, Stinger/POST CCMV Breadboard Guidance Assembly Tailor and Test Procedure, 5 May 1980, by W. O. Wilderson

APPENDIX A

OPERATION SEQUENCE FOR INSTALLATION OF THE STINGER/POST BREADBOARD INTO THE HYBRID SIMULATION

APPENDIX A

OPERATION SEQUENCE FOR INSTALLATION OF
THE STINGER/POST BREADBOARD INTO THE HYBRID SIMULATION

1. Check to ensure that the +5V, -5V, +20V, and -20V HISC-Breadboard power supplies are "Off".
2. Check to ensure that the HISC's patch panel is correctly patched.
3. Check to ensure that the HISC's power switch is "Off".
4. Connect the common wires from the HISC-Breadboard common bus to the Breadboard. Note that common is plugged into the black connector for the positive supply and the red connector for the negative supply.
5. Connect the +20V and the -20V power lines between the Breadboard and the power supplies.
6. Connect cable 1W6 between the BB I/O module of the HISC and the Breadboard. The nature of the connectors will prevent incorrect wiring. Connect the loose wire to J75 on the front panel of the Breadboard.
7. Check to ensure that the Breadboard's power switch is "Off".
8. Turn on the +5V, -5V, +20V, and -20V power supplies.
9. Turn "On" the HISC.

APPENDIX B

BREADBOARD PRECURSORY CHECKS REQUIRED FOR

MICOM SIMULATION

APPENDIX B
BREADBOARD PRECURSORY CHECKS REQUIRED FOR
MICOM SIMULATION

I. Initial Power-Up

Purpose:	Verify proper supply currents.
Initial Conditions:	Not critical
Monitor Signals:	Ammeters on Breadboard front panel.
Procedure:	<ol style="list-style-type: none">1. Turn "On" Breadboard.2. Observe ammeters; and if either indicates greater than one amp, turn "Off" Breadboard.3. Check wiring of power to Breadboard if needed.

II. Regulator Measurement

- Purpose: Verify voltage regulator potentials.
- Initial Conditions: Don't care.
- Monitor Signals:
- +15 Volt Regulator (J6 Front Panel)
 - 15 Volt Regulator (J8 Front Panel)
 - +10 Volt Regulator (J78 Front Panel)
 - +15 Volt Preamp Regulator (J37 Front Panel)
 - 15 Volt Preamp Regulator (J38 Front Panel)
- Procedure:
1. Check the monitor points for the correct potentials and institute repairs if needed.

III. Gyro and Secondary Speed Control, Caging, and Launch Function Verification

Purpose: Verify proper operation of the gyro and secondary speed control loops along with the associated caging and launch processes.

Initial Conditions: On/Off = On
Cage/Uncage = Caged
FOV = Enabled
AGC = Enabled
Launch = Pre-Launch
Target = C-IR
Look Angle = 0
Roll Rate = 0
Track Rate = 0

Monitor Signals: Precession (Analog Patch Panel)
Cage (Analog Patch Panel)
Gyro Drive (Analog Patch Panel)
Secondary Drive (Analog Patch Panel)
Gyro Reference (Analog Patch Panel)
Secondary Reference (Analog Patch Panel)

III. Gyro and Secondary Speed Control, Caging, and Launch Function Verification (Continued)

Procedure:

1. Initiate the gyro model operation with FF 010 on the analog console.
2. Check for the proper (while caged) gyro and secondary frequencies on the reference signals. Note that these frequencies are classified numbers.
3. If the secondary speed control loop is enabled, check to ensure that the reference follows the drive by 90° and that the drive signal is not saturated.
4. Check the caging action by uncaging and observing the cage coil signal. Some non-zero sine wave should develop. Caging should cause the precession command to drive the cage coil signal to zero.

III. Gyro and Secondary Speed Control, Caging, and Launch Function Verification (Continued)

5. Post launch status of the gyro speed control should be checked by observing the drive signal. It should not be saturated and held at a gyro spin plus roll frequency. Secondary drive should not be saturated and held at a secondary spin minus roll frequency. Additionally, gyro reference should follow drive by 180° and secondary reference should follow drive by 90° .

APPENDIX C

BREADBOARD TAILORING PROCEDURES REQUIRED FOR
MICOM SIMULATION

APPENDIX C
BREADBOARD (BB) TAILORING PROCEDURES REQUIRED FOR
MICOM SIMULATION

I. Scan Phase Tailor

Purpose: Tailor the electronics to match the seeker scan vector phase.

Initial Conditions:

On/Off	=	On
Cage/Uncage	=	Caged
FOV	=	Enabled
AGC	=	Enabled
Launch	=	Pre-Launch
Target	=	C-IR
Look Angle	=	0
Roll Rate	=	0
Track Rate	=	0

Monitor Signals:

CFAR Indicate (J56 - BB Front Panel)

IR Predetect (J5 - BB Front Panel)

Procedure:

Adjust the left DIP switch on CCA No. 4 (15V/128 bits - MSB on bottom) so that the IR Predetect Pulses are phased midway between the CFAR Indicate Signals.

II. Signal-to-Noise Ratio Adjustment

Purpose: Put AGC 6 dB down in the CFAR region.
(Initially tailors pulse amp about 2 dB below what noise number should be.)

Initial Conditions: On/Off = On
Cage/Uncage = Caged
FOV = Enabled
AGC = Enabled
Launch = Pre-Launch
Target = C-IR
Look Angle = Out of FOV
Roll Rate = 0
Track Rate = 0

Monitor Signals: IR Predetect (J5 - BB Front Panel)
JV Predetect (J20 - BB Front Panel)
IR/UV AGC Display

IR Procedure:

1. Adjust noise to -6 dB from FF
(.44 dB/step→F3) as indicated by
the "IR/UV AGC" display when switched
to "IR". IR Predetect approximately
250 mV noise.
2. Switch the "AGC" switch to "Hold".

II. Signal-to-Noise Ratio Adjustment (Continued)

IR Procedure:

3. Move the target to a 0° look angle.
4. Adjust the target intensity to 1.25 Vpk.

* UV Procedure:

1. Adjust noise to -6 dB from FF (.44 dB/Step \rightarrow F3) as indicated by the "IR/UV AGC" switch when switched to "UV". UV Predetect approximately 250 mv noise.
2. Switch the "AGC" switch to "Hold".
3. Move the target to a 0° look angle.
4. Adjust the target intensity to 2.5 Vpk.

* Reestablish initial conditions before performing UV procedure.

III. Track Phasing Tailor

Purpose: Tailor the phase of the synthesized error signal.

Note: Three methods are presented. Method III is coarse and should only be used if Methods I and II are ineffective. Method III should always be followed by Method I or II as a fine adjustment. Methods I and II are similar with Method II being recommended for general use.

Method I

Initial Conditions:	On/Off	=	On
	Cage/Uncage	=	Caged
	FOV	=	Enabled
	AGC	=	Enabled
	Launch	=	Pre-Launch
	Target	=	C-IR
	Look Angle	=	0
	Roll Rate	=	0
	Track Rate	=	0

Monitor Signals:	E_x (CCA No. 4 - U47 - Pin 7)
	E_y (CCA No. 4 - U48 - Pin 7)

III. Track Phasing Tailor (Continued)

Procedure:

1. Move target to .5 - .7 degrees off boresight in the horizontal plane.
2. Switch "Cage/Uncage to "Uncage".
3. Adjust the right DIP switch on CCA No. 4 (MSB = 180° - MSB on bottom) so that E_y has a zero value during the seeker's movement to the target.
4. Repeat Steps 3 and 4 until the condition in Step 4 is maintained.

Method II

Initial Conditions:

On/Off	=	On
Cage/Uncage	=	Uncaged
FOV	=	Enabled
AGC	=	Enabled
Launch	=	Pre-Launch
Target	=	C-IR
Look Angle	=	0
Roll Rate	=	0
Track Rate	=	3°/sec
J90-Front Panel	=	Logic 1 (Type 1 logic)

III. Track Phasing Tailor (Continued)

Monitor Signals: E_x (CCA No. 4 - U47 - Pin 7)

E_y (CCA No. 4 - U48 - Pin 7)

Procedure: Adjust the right DIP switch on CCA No. 4
(MSB = 180° - MSB on bottom) so that E_y
maintains a zero pointing error.

Method III

Initial Conditions: On/Off = On
Cage/Uncage = Uncaged
FOV = Enabled
AGC = Enabled
Launch = Pre-Launch
Target = C
Look Angle = .7 degree in horizontal
plane.
Roll Rate = 0
Track Rate = 0
J90-Front Panel = Logic 1 (Type 1 Logic)

Monitor Signals: Precession (J31 Front Panel)
Cage Coil (J32 Front Panel)

III. Track Phasing Tailor (Continued)

Procedure:

1. Move the target to a small pointing error in the same plane as the look angle.
2. Adjust the right DIP switch on CCA No. 4 (MSB = 180° - MSB on bottom) so that there is 0° phase error between Precession and Cage Coil at 105 Hz.

Note: If Precession and Cage are more than 30-40 degrees out of phase, the seeker will not track.

APPENDIX D

HYBRID SIMULATION INTEGRATION PLAN

APPENDIX D

HYBRID SIMULATION INTEGRATION PLAN

D.1 HYBRID SIMULATION INTEGRATION PLAN OVERVIEW

The recent availability of the required components with a defined status for each allows the definition of an orderly process to integrate the simulation in preparation for validation and subsequent prediction and analysis of missile flight performance. This plan is the definition of the intended procedure and includes descriptions of the tasks to be accomplished and descriptions of component status to the extent known. Some of the consequences of lack of component status definition will be addressed at least in terms of validation procedures. Future activities also will be identified to extent now possible.

This plan was prepared in February 1981 as the initial step of the integration. It was recognized that some of the real problems to be encountered certainly are not defined here and cannot be until actual use, validation and interfacing of the components. The plan will be updated by section as required to continue its usefulness as well as serve as a record of the process of integration. A separate integration report will be prepared following the initiation of sweep test validation.

D.2 STATUS OF INTEGRATION COMPONENTS

The collection of components needed for the simulation is now complete. The Guidance Electronics Breadboard has been delivered by the missile contractor, the ETSG has been demonstrated, the analog models are settled and the digital programs are available for open and closed loop use. Each component is described in Sections D.2.1 through D.2.3 in terms of its status relative to that required for integration.

D.2.1 Guidance Electronics Breadboard

The Breadboard will require very little validation and characterization because of the extensive experience the missile contractor has with this Breadboard. Recent availability of some operating instructions from the contractor which identifies displays and interprets significant display values will support checkout and scan and track phase tailoring as soon as the gyro and seeker signals are available.

D.2.2 Electronic Target Signal Generator

The ETSG has been demonstrated with several targets in both channels. Recent experience during checkout indicates that the unit is sufficiently reliable to support integration. The software is sufficiently understood to allow target generation.

Some features of the ETSG were demonstrated but the entire signal path was not exercised.* The analog seeker output and response to preamp gain switching were yet to be demonstrated.* The relation between target size and pulse width and between target intensity and pulse height must be determined. This can proceed when the analog gyro output becomes available. Several test circular targets and a nominal seeker must be characterized before the pulse output can be evaluated.

The Display CPU could not be used in real-time operation, but this was not regarded as critical because the diagnostic target map display was functional. A problem could occur if use of the Display CPU were attempted because nonrecoverable errors would occur requiring re-initialization of the ETSG.

D.2.3 Analog Program

The analog program had been compiled in ECSSL and was ready for patching.* A certain amount of lead time was lost because the analog program was moved from the AD-4 to the EAI 781 analog computer. An advantage of the latter is the similarity to the analog implementation of the missile contractor; a potential disadvantage was the required sharing of the 781 with other programs.

* These milestones were accomplished in March 1981.

The control logic has been patched and checked out.

Additional analog capability was implemented to provide prelaunch body rates simulating launcher motion caused by the gunner tracking a target between acquisition and boreclear. These additions probably are not required for initial closed-loop operation but will be needed for inner boundary definition.

Changes were required to provide the g-sensitive drift term to the analog gyro model, lead and superelevation ramped values of body attitude, and prelaunch constant potentiometer settings defining body rates in pitch and yaw to be active from Uncage to Boreclear. (The Analog Controller will set the potentiometers.)

D.3 INTEGRATION PROCEDURE

Several tasks were required to be accomplished before integration could be completed: the ETSG transfer functions must be characterized, some modifications to the Hybrid Interface Signal Conditioner (HISC) were required, breadboard power supplies must be installed and component signal functional interfaces must be validated.*

* This was accomplished in May 1981.

Significant events in the integration procedure are Plug-Up and Closed-Loop. Following interface validation and the above mentioned electrical modifications, the components were plugged up and open-loop characterization was to be accomplished, culminating in operation of the digital and analog programs in a short closed-loop with the ETSG and Breadboard operating in a monitor mode, with full-up closed-loop operation shortly following.

D.3.1 ETSG Characterization

D.3.1.1 Seeker/Target Build-Up

No simulation components other than the ETSG were involved in this task. A nominal model of a Stinger/POST seeker will be constructed and A and B circular targets will be loaded. Easily said, the procedure could be fairly lengthy because it is the first of its kind.

D.3.1.2 Seeker Audio Validation

The ETSG will require Cartesian rosette signals from the analog program and DCB information from the digital program for at least some part of this task. The A target will be positioned on boresight with the rosette running and the pulse sizes and shapes will be monitored. The atmospheric attenuation will be nulled. Initial ranges will be selected to simulate acquisition and the range will be decreased uniformly to half its

value to evaluate pulse width and amplitude functions. If range and pulse width scaling appears to be proper, the range will be halved again, and so on to the point where the target, which was an A at acquisition, fills the FOV. The range will be passed at the predetermined point where a B is reproduced to compare size and pulse output values with expected values. Intensity and pulse amplitude will be evaluated in D.3.1.3.

D.3.1.3 Range/Intensity Function Validation

The sequence identified in D.3.1.2 will be updated with a design atmospheric attenuation coefficient. Range effects on intensity will be evaluated.

D.3.2 Plug-Up Preparation

These tasks are basic to the functioning of the simulation but do not involve evaluation. All design has been accomplished.

D.3.2.1 HISC Interface Modification

The HISC was designed and assembled last year to interface with a nominal Guidance Electronics Breadboard. The actual Breadboard delivered at MICOM had been modified to simplify the interfaces required for simulation. Basically, current mode interfaces had been replaced by high-impedance voltage signals. The changes required in the HISC are identified

and not complex. This task is identified only because it must be accomplished.

D.3.2.2 Breadboard Cable Build-Up

A cable is required between the HISC and the Breadboard.* Connectors and wire are available and design was completed last year.

D.3.2.3 Breadboard Power Supply Installation

The power supplies for the Breadboard are to be installed in the ETSG cabinetry.** Installation has not been possible until recently because they have only lately been delivered. A variable supply had been borrowed to allow use of the Breadboard pending availability of the permanent supplies so that testing could have proceeded in their absence.

D.3.3 Analog Program Validation and Interface Checkout

The validation of the analog program is not unlike that required for any analog simulation. It would have been already accomplished if the analog program had not been moved to the EAI 781. As identified in the program status, some features are being added but these are not pivotal to early closed-loop operation.

* This cable was completed in March 1981.

** Power supplies were installed in March 1981.

D.3.3.1 Control Logic Interfaces

The interfacing of the control logic with the digital program is imminent.* The logic design is several months old and no problems are anticipated.

D.3.3.2 Gyro Model and Interfaces

The Stinger/POST gyro is functionally similar to that in Stinger but several characteristics and signal requirements are different and must be evaluated interconnected with the ETSG and Breadboard.

D.3.3.2.1 Damping Consideration

The damping coefficient is significantly different from that of Stinger. To remove some uncertainty of operation, the gyro will be characterized with both Stinger and POST damping values and will probably be operated initially with Stinger damping values.

D.3.3.2.2 ETSG Interface

The gyro model will provide Cartesian coordinates as function of gyro spin and secondary spin frequencies to the ETSG. The only unknown to be validated is the signal scaling for the ETSG input.

* This was complete in March 1981.

D.3.3.2.3 Digital Program Interface

The gyro model will require missile body pitch and yaw angles, angular rate and g-sensitive drift terms from the digital program.* When the digital idealized seeker is used for short closed-loop, precession will be commanded from the digital program. Also required will be the prelaunch body-rate constants for pot settings. The gyro model will provide look angle and cage coil values to the digital program. These interfaces will be checked with a simple open-loop digital program.

D.3.3.2.4 Breadboard Interface

Gyro drive commands will be provided by the breadboard along with precession, and the gyro will respond with reference and cage coil values. The interface validity will be evaluated following Breadboard scanned track phase tailoring with the ETSG providing seeker output to the Breadboard in response to an open-loop digital program.

D.3.3.3 Servomechanism Interface

The servomechanism model is well documented with test data and the AD-4 implementation had been validated.

* This was implemented in March 1981.

D.3.3.4 Ideal Seeker Validation

A rudimentary ideal seeker is provided in the analog program to provide precessions and steering commands in response to target indications from the digital program. This model will allow for checkout in the absence of valid Breadboard and ETSG signals. The model has already been operated in the AD-4 implementation.

D.3.4 Digital Program

The digital program is the central portion of the hybrid simulation. Only very limited checkout can be accomplished without it.

D.3.4.1 Open-Loop Validation

The digital program will provide open-loop support for ETSG characterization by varying target ranges, for Breadboard tailoring by positioning the target selectively within the FOV and for initial sweep tests using the A and B targets.

D.3.4.2 Short-Loop Operation

The digital program will be used to fly intercepts using either the digital or analog ideal seekers while providing target information to the

ETSG. The Breadboard output will be monitored and recorded but not used for wing commands.

D.3.4.3 Target Support

The digital program in a non-real-time environment will provide variable and varying aspect and orientation values desiring ETSG checkout.

D.3.4.4 Timing Consideration and Adjustment

The amount of timing delay around the closed-loop will be determined and must be compensated for in the digital program. Although several approximations and extrapolation methods can be defined, the problem will be illustrated with only one. The airframe will be rotated and translated as required rotation resulting from by the wing angle and thrust and drag tables. The targets in the FOV will be located by target inertial position and gyro line of sight (LOS). The problem arises from the signal transmit time in the ETSG. The analog pulses representative of a target scene are available from the ETSG from 2.7 to 5.7 ms after the DCB transmits the target description to the ETSG. This may require an extrapolation of gyro angle by 6.2 ms on the extrapolation of the gyro by some lesser amount and the extrapolation of wing angle. The gyro damping factor must be considered: the lower the damping, the less stable the extrapolation of gyro angle.

Multiple runs to determine the overall ETSG/Breadboard signal delay will be required in the short-loop mode (Section D.3.4.2).

D.4 SCHEDULE

The procedures and tasks described in Section D.3 will be implemented to accomplish initial Closed-Loop operation (Figure 4-1). The ETSG was capable of accepting seeker and target information and Cartesian target scan input, and provided analog pulses at the output resembling seeker output. Required maintenance or additional development on the ETSG could impact the schedule. Another critical item was the availability of the analog program, scheduled for close of business, 2 March 1981.* This will allow Breadboard checkout and phase tailoring, and analog-digital short-loop operation with the ETSG and Breadboard in a monitor mode.

Subsequent effort will involve preparation for static-gain curve characterization. This includes the development and tailoring of targets to match static gain curves to be provided in the Sweep Test Correlation Report. The same target models will then be applied to Sled Test scenarios.

* The program was available on time but not in a verified condition.

In parallel to this effort, flare control logic will be developed and implemented in the digital software. Loop time delays will be measured and digital software will be modified to compensate for the delay. Closed-Loop operations with simple and complex targets will be required for all the above tasks.

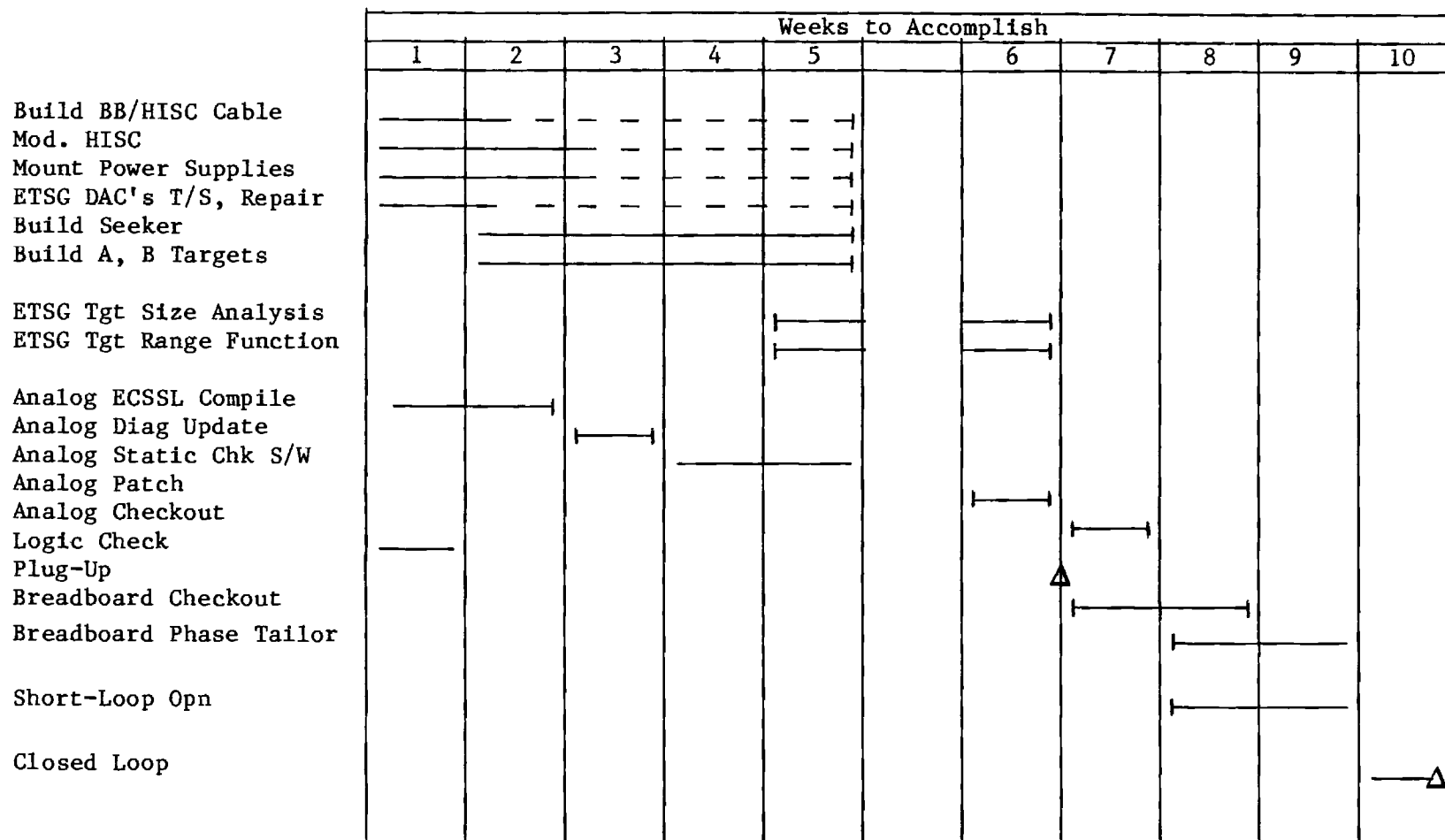


Figure 4-1. Integration Schedule

23 Feb 81